

AMENDMENTS TO THE CLAIMS

Please cancel claims 58-99.

LISTING OF CLAIMS

Claims 1-39: (Cancelled.)

40.(Previously Presented) A nonvolatile memory system comprising:
a nonvolatile memory including a plurality of nonvolatile memory cells and a shift register;
and
a control device coupled to said nonvolatile memory, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memory,
wherein said nonvolatile memory is enabled to operate a program operation,
wherein in said program operation, said nonvolatile memory receives said data from said control device, stores said data to said shift register and stores said data in said shift register to ones of said nonvolatile memory cells,
wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memory is operating in said program operation, and
wherein said shift register has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

Claims 41-46: (Cancelled.)

47.(Previously Presented) A nonvolatile memory system according to claim 40,
wherein said nonvolatile memory includes a plurality of word lines and a plurality of data lines, and wherein each of said nonvolatile memory cells is arranged at a crossing point of a corresponding one of said word lines and a corresponding one of said data lines and is coupled to the corresponding word line and corresponding data line.

48.(Previously Presented) A nonvolatile memory system according to claim 47,

wherein said nonvolatile memory includes a plurality of sectors each comprising one word line and ones of the nonvolatile memory cells coupled thereto, and wherein said shift register has a data storing capacity enabling the receiving of a unit of data of a length equal to the data storing capacity and enabling the storing of a unit of data in said sector.

49.(Previously Presented) A nonvolatile memory system according to claim 48, wherein said nonvolatile memory is a flash memory.

50.(Previously Presented) A nonvolatile memory system according to claim 40, wherein said control device includes a host interface comprised of a data bus transceiver, an address bus driver, an address decoder and a control bus controller, to enable communication between the nonvolatile memory and an external system bus.

51.(Previously Presented) A nonvolatile memory system comprising:
a plurality of nonvolatile memories each including a plurality of nonvolatile memory cells and a shift register; and
a control device coupled to said nonvolatile memories, wherein said control device is enabled to receive data from outside of said nonvolatile memory system and to apply said data to said nonvolatile memories,
wherein said nonvolatile memories are enabled to operate a program operation,
wherein in said program operation, each of said nonvolatile memories selectively receives said data from said control device, stores said data to said shift register thereof and stores said data in said shift register to ones of said nonvolatile memory cells of that nonvolatile memory,
wherein said control device is enabled to receive data from outside of said nonvolatile memory system, while said nonvolatile memories are operating in said program operation, and
wherein said shift register has a data storing capacity enabling the transfer of a unit of data of a length equal to the data length of said data to be stored at one time of said program operation, said data length being more than 1 byte.

Claim 52: (Cancelled.)

53.(Previously Presented) A nonvolatile memory system according to claim 51,
wherein each of said nonvolatile memories further includes a plurality of word lines and
a plurality of data lines, and

wherein each of said nonvolatile memory cells in each of the nonvolatile memories is arranged
at a crossing point of a corresponding one of said word lines and a corresponding one of said data
lines and is coupled to said corresponding word line and corresponding data line.

54.(Previously Presented) A nonvolatile memory system according to claim 53,
wherein each of said nonvolatile memories includes a plurality of sectors each comprising
one word line and ones of the nonvolatile memory cells coupled thereto, and

wherein said shift register has a data storing capacity for receiving data in units of a sector
and enabling the storing of a unit of data in said sector.

55.(Previously Presented) A nonvolatile memory system accordance to claim 54,
wherein each of said nonvolatile memories is a flash memory.

56.(Previously Presented) A nonvolatile memory system according to claim 55,
wherein said control device includes a host interface comprised of a data bus transceiver,
an address bus driver, an address decoder and a control bus controller, to enable communication
between the nonvolatile memories and an external system bus.

57.(Previously Presented) A nonvolatile memory system according to claim 51,
wherein said control device includes a host interface comprised of a data bus transceiver,
an address bus driver, an address decoder and a control bus controller, to enable communication
between the nonvolatile memories and an external system bus.

58-99.(Cancelled)